DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

University College of Engineering (Autonomous), Osmania University, Hyderabad - 500 007

Academic year 2020-2021

Class: B.E (CSE) -VI Semester

OFFLINE LABORATORY TIME TABLE

Date	10:00 to 13:00	14:00 to 17:00
Wednesday 1-09-2021	Introduction to Compiler Design (MVD/AG/DSK/) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Introduction to Computer Networks (LKSK / VS/ PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Thursday 02-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS / PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Friday 03-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS /PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Saturday 04-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS/ PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Monday 06-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS / PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Tuesday 07-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS / PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Wednesday 08-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS / PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab
Thursday 09-09-2021	Compiler Design (MVD/AG/DSK) Batch – I SW - I Lab, Batch – II R & D Lab –I Batch – III Room No. B-209	Computer Networks (LKSK / VS / PN) Batch – I SW – II Lab, Batch – II SW-III Lab & Batch – III SW – IV Lab

PRACTICALS

1. CD Lab – Compiler Design Lab
2. CN Lab – Computer Network Lab

LIST OF FACULTY

1.MVD – Mr.M.Venkat Dass / AG –Mrs.A.Gayathri / DSK – Mr.D.Sai Kumar
2.LKSK- Mr.L.K.Suresh Kumar / VS – Mrs.V.Sukanya / PN – Mr.P.Narayana

Batches

Batch – I (Roll Nos. 1005-18-733002 to 029)
Batch-II (Roll Nos. 1005-18-733030 to 056)
Batch-III (Roll Nos. 1005-18-733057 to 92)

B.E Time Table Incharge

HEAD
Department of
Computer Science & Engineering
College of Engineering, Osmania University

Head, Dept. of CSE.

Overall Time Table Incharge

Principal